REMARKS

Claims 1, 5, 6, 8, 10, 13, 14, 16, 19 and 20 have been amended. Claims 1, 3-8, 10-14, and 16-22 are the pending claims in this application.

Attached is a marked-up version of the changes being made by the current amendment.

Applicant asks that all claims be examined. No fee is due at this time. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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Version with markings to show changes made

In the claims:

Claims 1, 5, 6, 8, 10, 13, 14, 16, 19 and 20 have been amended as follows:

-- 1. (Twice amended) A computer system comprising:

a processor;

a memory unit configured to store data used by the processor;

a memory control unit configured to manage data flowing into and out of the memory unit;

a circuit board [having multiple layers and] comprising:

at least two layers formed in parallel to a surface of said circuit board,

a first signal line, formed on a first layer of the circuit board and connected between a first connection on the memory unit and the memory control unit; and

a second signal line also formed on the first layer of the circuit board and connected to the first connection on the memory unit, a first portion of the second signal line substantially parallel to a first portion of the first signal line, a second portion of the second signal line at an acute angle relative to a second portion of the first signal line,

wherein the widths of the lines and the distance separating the lines are each substantially equal, and

wherein said first layer defines a non-grounded gap between said first and second lines

5. (Three times amended) The system of claim 4, wherein the first signal line and the portion of the second signal line

that is routed substantially parallel to the first signal line are separated by a distance [about] substantially equal to said widths.

6. (Twice amended) The system of claim 5, wherein the widths of the lines and the distance separating the lines are each substantially equal to [about] 5 mils.

8. (Twice amended) A method for use in routing signals between a memory unit and a memory control unit, the method comprising:

delivering a first signal over a first signal line [formed] on a first [selected] layer formed in parallel to a second layer on a surface of a multi-layer circuit board and connected between the memory control unit and on the memory unit;

delivering a second signal over a second signal line formed on the first [selected] layer of the circuit board and connected to the first connection of the memory unit, a first portion of the second signal line formed substantially parallel to a first portion of the first signal line, a second portion of the second signal line formed at an acute angle relative to a second portion of the first signal line, wherein the first and second portions of the first and second signal lines are substantially equal in width; and

separating said first and second signal lines without a ground connection therebetween.

10. (Twice amended) The method of claim 8, further comprising delivering another signal to said memory control unit on another parallel layer of the circuit board over portions of

the first and second signal lines that are not separated by any conductive traces.

13. (Twice amended) The method of claim 12, wherein delivering the first signal and the second signal include delivering the signals over portions of the first and second signal lines that are [about] substantially equal to 5 mils wide and that are separated by a distance substantially equal to [of about] 5 mils.

14. (Twice amended) A method for use in manufacturing a computer system, the method comprising:

forming at least two parallel layers [a multiple-layer] on a surface of a circuit board, with first and second signal lines on a selected layer of the board;

connecting a memory unit to the board such that a first connection on the memory unit connects to the first and second signal lines;

affixing a memory control unit to the board such that the memory control unit connects to at least the first signal line;

forming a first portion of the second signal line to be substantially parallel to a first portion of the first signal line; and

forming a second portion of the second signal line to be at an acute angle relative to a second portion of the first signal line,

forming the first and second portions of the first and second signal lines substantially equal in width.

16. (Twice amended) The method of claim 14, further comprising forming the first and second signal lines such that

no conductive trace lies between the first signal line and the first portion of the second signal line that is routed substantially [roughly] parallel to the first signal line.

19. (Twice amended) The method of claim 18, further comprising forming the signal lines such that the widths of the lines and the distance separating the lines are all substantially [about] equal to 5 mils.

20. (Twice amended) A circuit board comprising at least two layers formed in parallel to a surface of said circuit board for use in a computer system comprising:

a memory unit;

a memory control unit; and

a data bus connecting the memory control unit to the memory unit and comprising:

a first signal line formed on a first [selected] layer of the circuit board and connected to the memory control unit and to a first connection on the memory unit; and

a second signal line formed on the first [selected] layer of the circuit board and also connected to the first connection on the memory control unit, a first portion of the second signal line substantially parallel to a first portion of the first signal line, a second portion of the second signal line at an acute angle relative to a second portion of the first signal line,

wherein the widths of the lines and the distance separating the lines are each substantially equal, and

wherein said first [selected] layer defines a non-grounded gap between said first and second lines. --